

A METHOD OF FORMING A RECESSED BURIED-DIFFUSION DEVICE

FIELD OF THE INVENTION

The present invention relates generally to semiconductor devices and more specifically to MOSFET gate devices.

BACKGROUND OF THE INVENTION

Prior devices employ a silicon nitride (SiN) spacer with a Co salicide scheme however this leads to high sheet resistance due to design rule limitation.

U.S. Patent No. 6,498,067 B1 to Perng et al. describes a process for forming a composite insulator spacer on the sides of a MOSFET gate structure.

SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide a method of forming a MOSFET gate device having a recess buried diffusion and the device so formed.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure having a gate structure formed thereover is provided. Respective low doped drains are formed within the structure at least adjacent to the gate structure. A pocket implant is formed within the structure. The structure adjacent the gate structure is etched to form respective trenches having exposed side walls. Respective first liner structures are formed at least over the exposed side walls of trenches. Respective second liner structures are formed over the first liner structures. Source/drain implants are formed adjacent to, and outboard of, second liner structures to complete formation of device.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 6 schematically illustrates a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Initial Structure – Fig. 1

As shown in Fig. 1, structure 10 includes a gate structure 18 with underlying gate oxide layer 16 with isolation structures 12, 14 on either side of the gate structure 18.

Structure 10 is preferably a silicon or germanium substrate and is more preferably a P⁺ silicon semiconductor substrate as shown in Fig. 1.

Gate structure 18 is preferably comprised of N⁺ polysilicon (N⁺ poly), polysilicon (poly) or tungsten silicide (WSi_x) and is more preferably N⁺ poly as shown in Fig. 1. Gate structure 18 has a thickness of preferably from about 1000 to 3000Å and more preferably from about 1500 to 2500Å. Poly gate structure 18 is preferably formed by: poly deposition; poly lithography and poly etching.

Underlying gate oxide layer (GOX) 16 is preferably silicon oxide and has a thickness of preferably from about 15 to 80Å and more preferably from about 45 to 75Å.

Isolation structures 12, 14 are preferably shallow trench isolation structures (STIs) and are preferably comprised of oxide, silicon oxide or HDP oxide and are more preferably oxide.

Formation of LDDs 20, 22 and Pocket Implants 24, 25 – Fig. 2

As shown in Fig. 2, low doped drains (LDDs) 20, 22 are formed within substrate 10 adjacent gate structure 18 to a depth of preferably from about 100 to 500Å and more preferably from about 150 to 300Å. LDDs 20, 22 are preferably formed using a tilt implant process so they 'undercut' gate structure 18 by preferably from about 100 to 250Å and more preferably from about 120 to 200Å from the respective edges of gate structure 18.

While LDDs 20, 22 are illustrated as being N⁻, LDDs 20, 22 may be either N⁻ or P⁻.

The tilt implant process is conducted at an angle of preferably from about 15 to 75° and more preferably from about 30 to 60°.

Pocket implants 24, 25 is also formed within substrate 10 to a depth of preferably from about 200 to 400Å and more preferably from about 250 to 350Å. Pocket implants 24, 25 are preferably P⁺ pocket implants for NMOS and are formed to prevent device punch-through.

Self-Aligned Trench 26, 28 Etch and First Rapid Thermal Anneal – Fig. 3

As shown in Fig. 3, self-aligned trenches 26, 28 are etched into substrate 10/LDDs 20, 22 STIs adjacent gate structure 18 and STIs 12, 14. This etching process also thins gate structure 18 and STIs 12, 14 to form: thinned gate structure 18' having a thickness of preferably from about 800 to 2800Å and more preferably from about 1300 to 2300Å; and etched STIs 12', 14'.

Trenches 26, 28 are recessed as at 30 by preferably from about 50 to 200Å and more preferably from about 70 to 130Å beneath GOX 16.

This leaves remaining LDDs 20', 22' as shown in Fig. 3.

An optional first rapid thermal anneal (RTA) may then be performed, either before or after formation of self-aligned trenches 26, 28 at a temperature of preferably from about 800 to 1000°C and more preferably from about 850 to 950°C for preferably about 3 seconds and more preferably about 2 seconds.

Formation of Liner TEOS Structures 32, 34 – Fig. 4

As shown in Fig. 4, a layer of TEOS is formed over the structure of Fig. 4 and is then etched back to form liner TEOS structures 32, 34 over the exposed side walls 31, 33 of thinned gate structure 18', GOX 16 and trenches 26, 28. Due to the conformal deposition of the TEOS layer and subsequent etch back, TEOS

structures 32, 34 are formed only on the exposed side walls 31, 33 of thinned gate structure 18' et al.

Liner TEOS structures 32, 34 have a thickness of preferably from about 100 to 500Å and more preferably from about 150 to 300Å.

Liner TEOS structures 32, 34 serve as buffer layers to relieve stress between poly gate 18' and the subsequently formed silicon nitride spacers 36, 38 as described below.

Formation of Liner SiN Structures 36, 38 – Fig. 5

As shown in Fig. 5, a layer of silicon nitride (Si_3N_4 or SiN) is formed over the structure of Fig. 4 and is then etched back to form liner SiN structures 36, 38 over respective liner TEOS structures 32, 34. Due to the conformal deposition of the SiN layer and subsequent etch back, SiN structures 32, 34 are formed only on the TEOS structures 32, 34.

Liner SiN structures 36, 38 have a thickness of preferably from about 300 to 2500Å and more preferably from about 500 to 1500Å.

Liner SiN structures 36, 38 serve as spacers and may retard E-field and increase breakdown voltage..

Formation of Source/Drain Implants 40, 42, Second Rapid Thermal Anneal And Salicide Structures 44, 46, 48 – Fig. 6

As shown in Fig. 6, respective source/drain implants 40, 42 are formed within substrate 10 adjacent and outboard of liner SiN structures 36, 38 to a depth of preferably from about 300 to 3000Å and more preferably from about 300 to 2500Å.

Source/drain implants 40, 42 are preferably N⁺ implants for NMOS.

This leaves final remaining LDDs 20'', 22'' as shown in Fig. 6.

A (second) rapid thermal anneal (RTA) is also performed after formation of source/drain implants 40, 42 at a temperature of preferably from about 1000 to 1100°C and more preferably from about 1010 to 1090°C for preferably from about 5 to 30 seconds and more preferably from about 7 to 20 seconds.

Respective metal salicide structures 44; 46, 48 are then formed over: thinned gate structure 18'; and source/drain implants 40, 42 to a thickness of preferably from about 50 to 300Å and more preferably from about 100 to 200Å. Metal salicide structures 44; 46, 48 are preferably cobalt salicide (CoSi_x), nickel salicide (NiSi_x) or titanium silicide (TiSi_x) and are more preferably cobalt salicide (CoSi_x) or nickel salicide (NiSi_x).

This completes the formation of the recessed buried-diffusion device
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Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1. reduction of RsBD (buried diffusion for drain side) and RsBS (buried diffusion for source side):
 - a. increase effective diffusion area due to minimized spacer by recess process; and
 - b. helpful for window design rule, high density approach;
2. increase gate added breakdown
 - a. avoid gate-induced drain leakage (GIDL) (band to band) due to source/drain being far away from the gate edge; and
 - b. higher voltage (HV) device is applied as LCD TV driver due to BVDj (junction breakdown) - can achieve > 20V;
3. potential reliability
 - a. better gate oxide integrity (GOI) performance due to good gate oxide protection;
 - b. avoid hot carrier effect; and
 - c. good capability of spacer width uniformity control;
4. formation of a high voltage device and product; and

5. excellent reliability performance.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.